REMARKS

Claims 1, 13, and 18 have been amended. Claims 1-9, 11-14, 16-23 are currently pending in the present application. No new matter has been added. Reexamination and reconsideration of the application are respectfully requested.

REJECTION OF CLAIMS 1-9, 11-14, 16, 18-23 UNDER 35 U.S.C. 103(a)

Claims 1-9, 11-14, 16, 18-23 are rejected under 35 U.S.C. 103 for the reasons set forth on pages 7-9 of the Action. Specifically, claims 1-9, 11-14, 16, 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda (U.S. Pat. No. 5,832,281, hereinafter referred to as "Maeda" or "the Maeda reference") in view of Hidehiko et al. (JP 06052070A, hereinafter referred to as "Hidehiko" or "the Hidehiko reference") and Smith et al. (U.S. Pat. No. 5,167,024, hereinafter referred to as "Smith" or "the Smith reference").

The Action on pages 7 and 8 states that Maeda does not teach the state save being a scan-based state save and further does not teach stopping the clock. Hidehiko is cited for teaching a scan-based state-save. Smith is cited for teaching stopping the clock. The Action then states "it would have been obvious to a person of ordinary skill in the art at the time of the invention to use a scan-based state-save as the state save in Maeda because this would have provided a fast method of data evacuation." Moreover, the Action states, "it would have been obvious to stop the clock when powering down because this would have saved power and prevented wasting the clock signals being applied to powered down circuitry."

The rejections under 35 U.S.C. 103 are respectfully traversed, at least insofar as applied to the amended claims, and reconsideration and reexamination of the application is respectfully requested for the reasons set forth hereinbelow. Specifically, this combination is contested as improper for the reasons advanced below. Moreover, even if this combination were proper, which is not conceded, the resulting combination would still fail to teach or suggest the claimed invention.

EVEN IF PROPERLY COMBINED, THE MAEDA REFERENCE, HIDEHIKO REFERENCE AND SMITH REFERENCE FAIL TO TEACH OR SUGGEST THE SPECIFIC LIMITATIONS SET FORTH BY THE INDEPENDENT AND DEPENDENT CLAIMS

As advanced hereinbelow, the cited references are improperly combined. However, it is respectfully submitted that even if the Maeda reference, Hidehiko reference, and Smith reference were properly combined, which is not conceded, Maeda, whether alone or in combination with Hidehiko and Smith, fails to teach or suggest specific limitations recited by the claims.

Specifically, Maeda, whether alone or in combination with Hidehiko and Smith, fails to teach or suggest "wherein the switched power area includes an input for receiving a normal mode clock signal and at least one transistor that is manufactured with a sub-micron semiconductor manufacturing process," as claimed in claims 1, 13, and 18, respectively.

First, none of the cited references fairly teach the above-noted limitation. Furthermore, none of the cited references even identify the problem solved by the claimed invention. For example, the Maeda reference is directed to solving a very

different problem than the claimed invention. Maeda's problem is that when a user replaces the battery that powers an area, which stores suspend information (Col. 1, lines 18-25), and also powers the registers of the detection circuit (Col. 1, lines 26-30), the suspend information and other information regarding the states of the power switch and the suspend/resume switch are lost. The loss of this information leads to undesirable and unintended consequences. (Col. 1, lines 35-50) Consequently, the aim of the apparatus of Maeda is to prevent the undesirable and unintended phenomena the set forth in lines 37 to 50 of col. 1 when the battery is replaced. (Col. 1, line 55 to Col. 2, line 20) Stated differently, the Maeda invention "improves the reliability of an information apparatus at battery replacement."

Moreover, Maeda, whether alone or in combination with Hidehiko, fails to teach or suggest "an inactive state power reduction manager .. for receiving a sleep signal and responsive thereto for asserting a stop clock signal to stop a normal mode clock, for performing a scan-based state-save", "b) stopping a normal mode clock; c) performing a state save by employing the scan circuitry," and "an inactive state power reduction manager .. for receiving a sleep signal and responsive thereto for asserting a stop clock signal to stop a normal mode clock, for performing a scan-based state save of state information of the first integrated circuit and the second integrated circuit by using the test access port of the first integrated circuit and the second integrated circuit," as claimed in claims 1, 13, and 18, respectively.

The detection circuit 38 of Maeda does not fairly teach or suggest the inactive state power reduction manager as claimed because 1) detection circuit 38 is not

disposed in a constant power area and 2) operates in a very different manner than the inactive state power reduction manager as claimed. First, detection circuit 38 is not in a constant power area as claimed. Instead detection circuit 38 is coupled to an interruptible source of power 34 (e.g., battery), which is the very reason for the Maeda invention (see col. 1, lines 31-35).

Second, the detection circuit 38 does not perform a state save as argued by Action since the detection circuit 38 does not control the HDD 15, where the state information is stored (see col. 1, 18-20). Instead, Maeda appears to utilize software (e.g., operating system that executes on CPU 12) to perform a state save. As described in the Background of the current application (page 4, lines 5-8), there are significant drawbacks to relying on software to perform the state save.

Similarly, Hidehiko, as far as can be understood from the translated abstract and figures, does not appear to have anything to do with power conservation or power reduction. Instead, Hidehiko is directed to a device and method for data protection in integrated circuits. Specifically, the Hidehiko reference describes a counter 4 that counts a scan clock and outputs an address of an external memory 3 in which data outputted from an IC 2 is stored. The IC 2 outputs internal state data from a scan output terminal SO synchronized by a scan clock SC. This data is then stored into memory 3. When the power source is restored, internal state data is restored to the IC 2 from the memory 3.

Paragraph 2 of the Action cites paragraph 0005 of Hidehiko as expressly setting forth a motivation to combine Maeda with Hidehiko. Applicant is not in possession of

an English translation of the Japanese patent and instead only has a translation of the Abstract of the Japanese patent. A copy of the English translation on which the Examiner relies is respectfully requested.

It appears that Hidehiko does little more than to describe the use of scan signals to read data from an IC and to write data to the IC. Hidehiko does not appear to teach a power reduction mechanism as claimed. Furthermore, Hidehiko does not appear to teach that the IC includes a clock input that receives a normal clock signal as claimed. Moreover, Hidehiko does not appear to teach a power reduction mechanism that stops the normal clock signal as claimed.

Although the Smith reference is directed to managing power consumption and power conservation, Smith utilizes standard methods to save state information and fails to teach or suggest the claimed invention. The power manager of the Smith reference operates in one of the following modes: normal, slow and sleep. In the normal mode, "most of the units are active at all times and/or some of the other units are caused to be made active when needed. In the slow mode, the power manager decreases the frequency of the clock signals in order to decrease the power consumption. It is respectfully noted that the normal mode and the slow mode are not relevant to this discussion since power is not removed from the various units in the computer (i.e., no state save is required).

In the sleep mode, the "computer enters into an inactive state, and the power manager continues to monitor various circuit conditions." Sleep mode can be triggered by a low battery level or when no user activity is detected for a predetermined amount

of time. State save is performed prior to entering sleep mode. However, it is respectfully noted that Smith relies on the operating system and other software drivers to perform the state save. Smith states the following: "Before entering the sleep mode, the operating system of the computer, as well as the various drivers, save the current state information in RAM 14. Thus, the state of the various registers, drivers and other memory devices are stored within RAM 14 for later restoration." As noted on page 4, lines 5-8 of the Background of the current application, there are significant drawbacks to relying on software to perform the state save.

Moreover, it is respectfully submitted that Smith does not teach the stopping a system clock as part of saving state information as implied by the Action. Instead, when the power manager stops the clocks, it does not save state since the internal state is frozen. Specifically, Smith states:

> The internal clock of PMGR 11 can be decoupled from CPU 12 by clock control unit 27 thereby disabling the clock input to CPU 12 and halting the execution of the CPU. The CPU internal states are frozen with all CPU internal RAM and control registers remaining intact by halting the execution of the CPU. Halting the execution of CPU 12 typically will lower its power consumption by two orders of magnitude.

As described in the Background of the current application, the halting of the system clock is a prior art solution for circuits manufactured with greater than one micron processes. Unfortunately, this solution of halting the system clock is not a viable solution for circuits manufactured with sub-micron processes.

It is noted that the dependent claims incorporate all the limitations of independent claims 1, 13, and 18, respectively. Furthermore, the dependent claims also

add additional limitations, thereby making the dependent claims a fortiori and independently patentable over the cited references.

For example, dependent claims 21-23 recite limitations related to receiving a wake-up signal; responsive to the wake-up signal, re-connecting the switched power portion of the circuit to power; g) performing a state restore by employing the scan circuitry; and h) re-starting the normal mode clock. These limitations do not appear to be taught or suggested by the Maeda, Hidehiko and Smith references.

In view of the foregoing, it is respectfully submitted that the Maeda reference, whether alone or in combination with the Hidehiko and Smith references, fails to teach or suggest the circuit, method and circuit board as claimed. Accordingly, it is respectfully requested that the claim rejections under 35 U.S.C. Section 103(a) be withdrawn.

THE PROPOSED COMBINATION IS BASED ON IMPERMISSIBLE USE OF THE CLAIMED INVENTION AS A TEMPLATE TO PIECE TOGETHER THE TEACHINGS OF THE MAEDA REFERENCE, THE HIDEHIKO REFERENCE AND THE SMITH REFERENCE

It is respectfully submitted that the Maeda, Hidehiko, and Smith references are improperly combined. It appears that the Action uses improper hindsight to selectively pick teachings from Maeda, teachings from Hidehiko, and teachings from Smith to arrive at the claimed invention.

As advanced previously, none of the cited references sets forth or addresses the specific problem addressed by the current invention as set forth in the application. Maeda appears to be directed to improving the reliability of an information apparatus at battery replacement. Hidehiko is directed to an apparatus for protecting data loss.

Smith utilizes a power manager that has a normal mode, a sleep mode and a slow mode.

In sharp contrast, the invention as claimed provides power reduction management to address the problem of computing devices with transistors, manufactured with sub-micron processes, where it is no longer sufficient to simply stop the clock, but the chips must be completely disconnected from the power supply in order to conserve power as set forth in the specification. (Specification, pages 3-4)

Consequently, it appears that the current patent application has been improperly used as a basis for the motivation to combine or modify the components selected from Maeda, Hidehiko, and Smith to arrive at the claimed invention. Stated differently, the proposed combination of the cited references appears to be based on impermissible hindsight reconstruction.

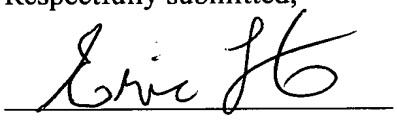
The Federal Circuit has held, "It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated, "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." (quoting In re Fine, 837 F.2d 1071, 1075, 5 USPQ 2d 1596, 1600 (Fed. Cir. 1988)), In re Fritch, 23 USPQ 2d 1780, 1784 (Fed. Cir. 1992). [emphasis added.]

In view of the foregoing, it is respectfully submitted that the Maeda reference, whether alone or in combination with the Hidehiko reference, fails to teach or suggest the circuit, method, and circuit board as claimed. Accordingly, it is respectfully requested that the claim rejections under 35 U.S.C. Section 103(a) be withdrawn.

Conclusion

For all the reasons advanced above, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the pending claims are requested, and allowance is earnestly solicited at an early date. The Examiner is invited to telephone the undersigned if the Examiner has any suggestions, thoughts or comments, which might expedite the prosecution of this case.

Respectfully submitted,



Eric Ho, Reg. No. 39,711
Attorney for Applicant
20601 Bergamo Way Tel: (818) 998-7220
Northridge, CA 91326 Fax: (818) 998-7242

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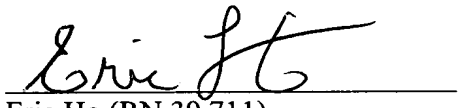

Eric Ho (RN 39,711) Nov. 19, 2004 (Date)